FORM PTO-1390 (REV 11-2000)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 124-865
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO (If known, see 37 C.F.R 1.5) 09/868242 Unknown
INTERNATIONAL APPLICATION NO. PCT/GB99/04277 ✓	INTERNATIONAL FILING DATE 16 December 1999 ✓	PRIORITY DATE CLAIMED 19 December 1998 ✓

TITLE OF INVENTION

FAST READOUT OF MULTIPLE DIGITAL BIT PLANES FOR DISPLAY OF GREYSCALE IMAGES

APPLICANT(S) FOR DO/EO/US

COKER et al Timothy Martin

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☐ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   - a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   - b. ☒ has been communicated by the International Bureau.
   - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   - a. ☐ is attached hereto.
   - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   - b. ☐ have been communicated by the International Bureau.
   - c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   - d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information. PTO-1449 and copy of International Search Report

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/868242 Unknown	PCT/GB99/04277	124-865

21. ☒ The following fees are submitted:

	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):	
-- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00	
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00	
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO $710.00	
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00	
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$ 130.00

CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE		
Total Claims	11	-20 =	0	X	$18.00	$ 0.00
Independent Claims	1	-3 =	0	X	$80.00	0.00
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)				$270.00		$ 270.00
					TOTAL OF ABOVE CALCULATIONS =	$ **1260.00**
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.						0.00
					SUBTOTAL =	$ **1260.00**
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)).					+	0.00
					TOTAL NATIONAL FEE =	$ **1260.00**
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property					+	$ 0.00
Fee for Petition to Revive Unintentionally Abandoned Application ($1240.00 – Small Entity = $620.00)						$ 0.00
					TOTAL FEES ENCLOSED =	$ **1260.00**
					Amount to be: refunded	$
					Charged	$

a. ☒ A check in the amount of $1260.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.
d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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Stanley C. Spooner
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27,393 **June 14, 2001**
REGISTRATION NUMBER Date

Method Of Signal Processing For Multi-Level Imaging

The present invention relates to a method of signal processing for multi-level, e.g.greyscale, imaging, and to using such a method for operating a display or spatial light modulator in which the instantaneous intensity distribution afforded by the display or modulator is binary in nature but which is altered in a manner such that the time averaged distribution effectively has, or appears to have, multiple intensity levels, e.g. of intensity. For display purposes, this means that the alteration must be sufficiently fast for averaging to occur at the eye, preferably avoiding any flicker. This requirement may or may not apply for other purposes.

The signal processing method of the invention can be used in conjunction with any spatial light modulator capable of producing a binary image, including those comprising an array of individually addressable cells or pixels, and those where the binary image is produced by scanning of a modulated light beam, for example. The term " binary spatial light modulator " used herein is intended to encompass all such devices, whether they are used for display or other purposes, for example information recordal, and variable components (for example lenses, filters and diffraction gratings) in optical systems. The term is intended to cover passive modulators where an existing light beam is affected by the modulator, and also those which act as light sources, for example arrays of light emitters, and electroluminescent devices.

The term "image" as used herein is used to denote any spatially varied light distribution, normally, but not necessarily, of light intensity, and its production or resulting distribution will be referred to by the term "display".

Furthermore, although the term "grey scale" is used herein as denoting a multi-level distribution, it should be made clear that the term is used in relation to any colour, including white. In addition, although the methods, arrays, backplanes, circuitry etc. of the invention and its embodiment are described in relation to a single colour (monochrome images), including white, it is envisaged that variable colour images or

displays etc. will be produced in manners known per se, such as by spatially subdividing a single array into different colour pixels, superimposing displays from differently coloured monochrome arrays for example by projection, or temporal multiplexing, for example sequential projection of red green and blue images.

Temporally varying binary modulation to achieve a multiple intensity effect is known, and can be effected by the use of multiple bit planes. In such a scheme, an array of digitised values, of amplitudes corresponding to the grey scale values allocated to the pixels of the array, is decomposed into a multiplicity of bit planes. This multiple bit plane technique may be used with any binary spatial light modulator as defined above.

It is possible to decompose a n-level digitised grey scale image into a plurality of image planes, or bit planes, e.g. binary planes (see below), of equal duration. However, in a preferred form, known as a weighted bit plane technique, the durations of the bit planes are weighted, each bit plane being representative of one level (exponent) of the digitisation. This reduces the number of bit planes which need to be stored to synthesise an image, and can reduce addressing requirements somewhat.

Although in certain cases, it would be possible to use digital bases other than 2, this complicates matters insofar as each bit plane is not binary and thus is not so easily stored. Furthermore, each location of such a bit plane would then have more than one non-zero value, and the variation in non-zero values across the bit plane would need to be taken into account for the durations of operation of each pixel (possibly by further decomposing the non-binary bit plane to two or more binary bit planes). The discussion below will be limited to binary weighting, but the principles set out in such a context are believed to be sufficient to enable the skilled person to extrapolate to other exponential bases if required or desired.

Where the digitisation is binary, so that each bit plane is an array of digital 1s and 0s, it is then only necessary to display each bit plane for a total period proportional to its binary weighting to provide a time averaged image equivalent to the digitised grey scale image.

Where possible, it is convenient to display each binary bit plane once for the total duration necessary to contribute to the grey scale image, but it is also possible to display one or more of the bit planes a plurality of times, not necessarily sequentially, provided that the total time spent in displaying each bit plane, relative to the total time spent in displaying all the bit planes, is proportional to its binary weighting.

The different bit planes for a grey scale image can be stored as sequential binary strings in a computer, and will be read out one at a time in any desired order after which they can be discarded unless the image needs to be repeated. It is computationally easiest to read out the bit planes in the order in which they have been stored, since then the only address which needs to be stored is the starting address of the first stored bit planes, all bit planes then being read out one at a time simply by clocking out a predetermined number of data bits in sequence for each bit planes.

It might be possible immediately to replace bit planes that have been read by the bit planes for a succeeding image, particularly where the bit planes are being produced in real time. However, under other circumstances this could be difficult, and the set of bit planes for a successive image will then normally be stored elsewhere. In certain cases it would be possible to provide storage for just two bit planes one of which is written while the other is being read, and vice versa.

It would also be possible to control the reading and/or writing processes so as to convert the image standards as desired, for example from line sequential to interlaced.

As or after each bit plane is read from memory, it is then written, e.g. using the single pass scheme described below, and viewed over a period corresponding to its weighting so that the eye synthesises the intended grey scale image. The single pass scheme is preferred insofar as it merely over-writes the preceding bit plane without the need for a second pass, the associated front electrode switching and blanking pulses. The avoidance of lost time between successive valid images enables continuous illumination and the easier provision of bit planes of an accurately weighted duration.

In such a scheme, each pixel is subjected to a series of voltage pulses according to the point in the grey scale it represents (as in the number representing the grey scale level, and usually but not necessarily in that order). There are more points in the grey scale than there are applications of voltages, due to the weighting employed, which is advantageous since it reduces the time spent actually driving the array. Each applied voltage may be of the same or opposed polarity compared to the preceding voltage, and the same number of voltage pulses, equal to the number of bit planes (ignoring polarity), is applied to each pixel to synthesise the image.

For example, in a 64 level grey scale with binary weighting, there will be 6 bit planes with relative durations of $2^n t$ where n ranges from 0 to 5, and each pixel can be represented by a corresponding 6 digit binary number.

However, double pass schemes below could alternatively be adapted for use in multiple or weighted bit plane schemes.

To achieve dc balance, it would be possible to produce each binary bit plane by any binary imaging method which itself produces dc balance - for example by starting from a blank image, writing, viewing and erasing the binary image by selective energisation (+V) and driven blanking (-V) of selected pixels only.

However, in most or all of such schemes, the actual duration of the binary image is not directly proportional to the time allocated thereto, for example because of intervening blanking steps, etc., leading to a degree of distortion in the binary nature of the bit plane periods, and hence the perceived grey scale values. While this could be compensated for if desired, it represents an additional complication.

Recently there has been developed a novel spatial light modulator in the form of a smectic liquid crystal layer disposed between an active semiconductor backplane and a common front electrode. It was developed in response to a requirement for a fast and, if possible, inexpensive, spatial light modulator comprising a relatively large number of pixels (320 x 240 up to 640 x 480) with potential application not only as a display device, but also for other forms of optical processing such as correlation and

holographic switching. Depending on the manner in which it is driven, and the value of the applied voltage, the modulator may be driven at a line rate of at least 10MHz and a frame rate of up to 15 to 20kHz, requiring a data input of around 1 to 1.5 Gpixel per second. Typically, while the pixel address time is around 100 nanoseconds, the pixel will actually take around 1 to 5 microseconds to switch between optical states; and while overall frame writing time is of the order of 24 microseconds, the frame to frame writing period is around 80 microseconds.

This spatial light modulator can be driven according to single pass schemes, in which the front electrode is placed at a potential of V/2 relative to the backplane pixels, which are switched to zero volts or V volts.

Alternatively it can be driven according to double pass schemes in which in one pass the front electrode is placed at zero volts and selected pixels are turned ON by switching pixel elements of the backplane array to V volts, and in the other pass the front electrode is placed at V volts and selected pixels are turned OFF by switching elements of the array to zero volts. For pixels which are not in the process of being switched the elements of the backplane follow the voltage of the front electrode. To maintain the same potential difference therebetween, the voltage at all backplane pixel elements of the array is simultaneously switched as the voltage on the front electrode is changed between zero and V volts.

Our copending International Patent Applications (PCT/GB99/04285, ref: P20957WO, priority GB9827952.4; PCT/GB99/04286 and PCT/GB99/04276, refs: P20958WO and P20958WO1, both priority GB9827965.6; PCT/GB99/04282, ref: P20959WO, priority GB9827900.3; PCT/GB99/04279, ref: P20960WO, priority GB9827901.1; PCT/GB99/04274, ref: P20961WO, priority GB9827964.9; PCT/GB99/04275, ref: P20962WO, priority GB9827945.8; and PCT/GB99/04260, ref: P20963WO, priority GB 9827944.1) relate to other inventive aspects associated with this spatial light modulator, including the single and double pass schemes referred to in the preceding paragraph.

The aforesaid spatial light modulator is ideally suited to the use of the bit plane technique mentioned above. However, the present invention is not limited to liquid crystal modulators, but can be applied to any spatial light modulator as referred to above.

One problem which arises, particularly when operating liquid crystal display and modulators, is that of maintaining a dc balance at individual pixels. Our copending International Patent Application (PCT/GB99/04260, ref: P20963WO) filed together with this application is directed to a weighted bit plane technique as described above in which at least some of the bit planes are modified, and relates to a method of grey scale imaging using a weighted bit plane technique, in which an n-digit binary number represents the intended grey level of each pixel location in an array of binary pixels, wherein at least one said binary number has an unequal number of 1s and 0s, said method comprising the step of altering the number to a closely adjacent value such as to reduce the inequality of 1s and 0s. That method has particular but not exclusive relevance to the production of effective grey scale intensity distributions for display purposes, where the effective duration of the binary images (length and/or number of repeats) is such that temporal integration thereof, for example by a viewer, gives the grey scale image. It finds particular but not exclusive application to liquid crystal spatial light modulators, and enables dc balance to be obtained or at least more closely approximated at each pixel.

The weighted bit plane method as operated therein requires that relaxation of the liquid crystal pixels is negligible over the duration of the longest bit plane, and this is not always possible. In such a case, the bit planes can be refreshed during the bit plane period(s), but at the expense of dc balance.

Basically, a refresh step comprises repeating the application of the same voltage as was applied at the start of the bit plane so as to restore the switched state of the pixel. It may even be that the nth power binary weighted bit plane needs to be refreshed (2^n-1) times subsequent to the first writing so that a 2^n greyscale will involve 2^n frame writes of binary images when the refresh writing stages are included.

In a refresh scheme, bit planes are read out more than once, depending on the duration thereof. Thus it is not possible to discard the bit plane until it has undergone its final reading. Furthermore, if each bit plane is repeatedly read for the requisite number of times before proceeding to the next bit plane, it is necessary to store the starting address of the two bit planes.

For example, taking a simple case of three bit planes A, B and C, of relative durations 4t, 2t and t respectively, it would be possible to read these out in the order AAAABBC. However, this necessitates storing the start addresses of each of the bit planes, apart from plane C which is read only once, in order that the correct place for the refresh readout may be reached.

European Patent Application 0762375 illustrates a method where bit planes are repeated a plurality of times according to their weighting, but the occurrences of the higher weighted bit planes are distributed throughout the display (frame) period. The bitplane sequence is not such that a lower weighted bit plane is always preceded by the next higher weighted bit plane, as will occur in the present invention to be explained below.

In addition, and perhaps more importantly, there are cases where it is necessary to rewrite the entire grey scale image before proceeding to a new image, where display times are long or relaxation is fast for example. In such a case it is necessary not only to store the start address of the bit plane next to be used, but also the start address of the first bit plane of the entire sequence, until that image information is no longer required.

An improved method of readout in such cases makes it possible to avoid the storage of a plurality of start addresses. At the high speeds involved in reading out the images when using the spatial light modulator of the preferred embodiment, this apparently minor step can be computationally significant and advantageous.

The present invention provides a method of image signal processing wherein a signal defining a pixellated multi-level image is defined by a first plurality of binary strings

in a memory, the strings having associated therewith respective weightings and defining respective bit planes each corresponding to a digitised pixelwise intensity distribution, such that the weighted pixelwise intensity distribution over all said plurality of bit planes corresponds to said multi-level image,

the method being characterised in that at least a second plurality of said binary strings associated with the highest weightings are stored in sequential locations in said memory in decreasing order of weighting and the method including the step of making a succession of read cycles from the stored strings, each read cycle consisting of reading one or more of the stored strings in sequence as stored, commencing with the string for the highest weighting, the numbers of the strings read in the read cycles being varied so that at the end of the said succession of read cycles each string of the second plurality has been read out a number of times proportional to its associated weighting.

Preferably the multi-level image is a multi-intensity image.

The said succession of read cycles is repeated, for example where display times are long or relaxation is fast as noted above.

In one form of the method according to the invention all of the first plurality of strings are stored in sequential locations in said memory in decreasing order of weighting. In this case the succession of read cycles can be such that each string of the first plurality is read out a number of times proportional to its weighting.

The invention extends to a method of imaging in which the method of signal processing according to the invention is performed and each string of the first plurality is displayed as its bit plane each time it is read during the succession of read cycles for substantially the same period.

In another form of the method of signal processing according to the invention there is at least one said string with lower weighting, in addition to said second plurality, which is read out once during said succession of read cycles. In this case the invention also extends to a method of imaging by performing such a method of signal

processing wherein each string of the first plurality is displayed as its bit plane each time it is read during the succession of read cycles for substantially the same period, wherein when it is read said at least one said string with lower weighting is displayed as its bit plane for a duration which is less than said period and proportional to its weighting relative to the weighting of the lowest order string of the second plurality.

In a preferred imaging method the bit planes are displayed on a pixellated liquid crystal display. A small ac potential difference may of signal processing applied to pixels of the liquid display in periods when bit planes are not being written.

Thus the present invention requires that the second plurality of the bit planes, or all the bit planes, are stored as binary strings in sequential locations in a memory in decreasing order of weighting. By cyclically reading out from the stored bitplanes in sequence, starting with the highest weighted plane but varying the number of planes actually read out in each cycle, each bit plane can be read out a plurality of times proportional to or equal to its weighting. Where there are lower weighted planes in addition to the second plurality, these will be read out once, for duration(s) less than the lowest order bit plane of the first plurality. This can be done at any time, including a period or periods within the reading out of the second plurality, but is preferably performed before or after the entire second plurality has been read.

Thus in a method according to the present invention the triple bit plane image exemplified above will be read out with read passes ABC (once), AB (once), and A (twice), which when combined can give an overall order, for example, of ABCABAA, or ABCAAAB or ABAAABC as desired. Only the start address needs to be stored since each read pass commences at the same place, and continues to an address determined by counters.

While some grey scale and refresh schemes automatically provide dc balance, a further option for schemes which do not do this is to allow dc imbalance to accumulate, for example while writing images and then allowing them to relax, calculating the imbalance (e.g. in an accompanying computer simulation), and then

applying local dc voltages to the pixels of a magnitude and duration such as to provide zero average dc.

It should be understood that there have been references above to a liquid crystal cell incorporating an addressable array, the methods of the invention may be used in relation to any binary spatial light modulator. Where the imaging device is a liquid crystal device, prolongation of the binary images used to synthesise the grey scale image may be achieved in known manner by the application of a small ac field between successive binary images.

CLAIMS

1. A method of image signal processing wherein a signal defining a pixellated multi-level image is defined by a first plurality of binary strings in a memory, the strings having associated therewith respective weightings and defining respective bit planes each corresponding to a digitised pixelwise intensity distribution, such that the weighted pixelwise intensity distribution over all said plurality of bit planes corresponds to said multi-level image,

the method being characterised in that at least a second plurality of said binary strings associated with the highest weightings are stored in sequential locations in said memory in decreasing order of weighting and the method including the step of making a succession of read cycles from the stored strings, each read cycle consisting of reading one or more of the stored strings in sequence as stored, commencing with the string for the highest weighting, the numbers of the strings read in the read cycles being varied so that at the end of the said succession of read cycles each string of the second plurality has been read out a number of times proportional to its associated weighting.

2. A method according to claim 1 wherein the multi-level image is a multi-intensity image.

3. A method according to claim 1 or claim 2 wherein the said succession of read cycles is repeated.

4. A method according to any preceding claim wherein all of the first plurality of strings are stored in sequential locations in said memory in decreasing order of weighting.

5. A method according to claim 4 wherein said succession of read cycles is such that each string of the first plurality is read out a number of times proportional to its weighting.

6. A method according to any one of claims 1 to 4 wherein there is at least one said string with lower weighting, in addition to said second plurality, which is read out once during said succession of read cycles.

7. A method of imaging comprising the steps of performing the method according to any one of claims 1 to 5 and displaying each string of the first plurality as its bit plane each time it is read during the succession of read cycles for substantially the same period.

8. A method of imaging comprising the steps of performing the method according to claim 6 and displaying each string of the first plurality as its bit plane each time it is read during the succession of read cycles for substantially the same period, wherein when it is read said at least one said string with lower weighting is displayed as its bit plane for a duration which is less than said period and proportional to its weighting relative to the weighting of the lowest order string of the second plurality.

9. A method of imaging according to claim 7 or claim 8 wherein the bit planes are displayed on a pixellated liquid crystal display.

10. A method according to claim 9 wherein a small ac potential difference is applied to pixels of the display in periods when bit planes are not being written.

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Fast Readout of multiple digital Bit planes for display of Greyscales Images

the specification of which (check applicable box(s)):

☐ is attached hereto

☐ was filed on _____ as U.S. Application Serial No. _____

☒ was filed as PCT international application No. PCT/GB99/04277 on 16/12/1999

and (if applicable to U.S. or PCT application) was amended on 25/01/2001

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
9827944.1	GB	19/12/1998

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT International applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT International filing date of this application:

Prior U.S./PCT Application(s):

Application Serial No.	Day/Month/Year Filed	Status: patented pending, abandoned
PCT/GB99/04277	16/12/1999	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And I hereby appoint NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed), and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27078; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr. 29366; Thomas E. Byrne, 32205; Mary J. Wilson, 32955; J. Scott Davidson, 33489; Alan M. Kagen, 36178; William J. Griffin, 31260; Robert A. Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331.*

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*OR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.